Tamarisk®320

17 µm 320x240 Long Wave Infrared Camera

Electrical Interface Control Document

Document No: 1012820

Revision: D

DRS Technologies

A Finmeccanica Company

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Rev History

Revision Number	Release Date	Description
A	01/24/2013	Initial Release
B	9/5/2013	Derived from Tamarisk 640 version
C	06/09/2014	Prepared for Public Release
D	2/15/2015	Updated PDVO Timing

Camera Link® is a registered trademark of the Automated Imaging Association.

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ACRONYMS AND ABBREVIATIONS

Abbreviation	Description	Abbreviation	Description
°C	Celsius	mm	millimeter
°F	Fahrenheit	ms	milliseconds
AGC	automatic gain control	MSB	Most Significant Bit
BPR	bad pixel replacement	MTU	Maximum Transfer Unit
CCA	circuit card assembly	MWIR	Mid-wave infrared
CL	center line	NETD	noise equivalent temperature difference
COMM	communication	NTSC	National Television System Committee
CSC	Computer Software Component	NUC	non-uniformity correction
CSCI	Computer Software Configuration Item	NVTHERM	Night Vision Thermal Analysis Tool
CSU	Computer Software Unit	OEM	original equipment manufacturer
dB	decibels	OLA	Optical Lens Adapter
DSP	digital signal processor	P	probability
ESD	electrostatic discharge	POL	polarity
E-Zoom	electronic zoom	psi	pound per square inch
FOV	field of view	Rev	revision
FPA	Focal Plane Array	ROI	region of interest
ft	feet	SC	split configuration
G	gravitational force	SWIR	Short-wave infrared
g	gram	TBD	To Be Determined
GUI	graphical user interface	TCR	Temperature coefficient of resistance
H	height	TIM	Thermal Imaging Module
HFOV	horizontal field of view	UART	Universal Asynchronous Receiver Transmitter
I/O	input/output	UAV	unmanned aerial vehicle
ICD	Interface Control Document	UFPA	Un-cooled Focal Plane Array
ICE	Image Contrast Enhancement	USB	Universal Serial Bus
ID	identification	V	Vertical or Voltage
IR	infrared	VDC	volts direct current
IRS	Interface Requirements Specification	VGA	video graphics array
km	kilometer	VOx	Vanadium Oxide
LR	lower right	W	width or Watt
LWIR	long-wave infrared	µm	micron (micrometer)

REFERENCE DOCUMENTATION

The following documents form part of this specification. In the event of a conflict between documents referenced herein and the contents of this specification, the contents of this specification shall be considered a superseding requirement.

Document No: 1012593 Tamarisk®320 User Manual

Document No: 1012819 Tamarisk®320 Software Interface Control Document

Document No: 1012821 Tamarisk®320 Camera Control Software User Guide

Document No: 1003727 Tamarisk®320 Mechanical Interface Control Document

SAFETY INSTRUCTIONS

NOTIFICATIONS: CAUTION, WARNING AND NOTE

The following is a list of notifications and their accompanying symbol that may be found throught this document to alert the reader to potential risks and to minimize the potential for personal injury and or damage to the product. When a notification is present, it is important that the user review and understand all statements related to the notification before proceeding. If questions arise, please contact your authorized dealler or DRS Technologies.

Notifications are preceeded by a symbol and followed by highlighted text. Three types of notifications are typically used and are defined below:

CAUTION

A caution is a procedure, practice, or condition that, if not strictly followed, may result in personal injury or damage to the equipment that may impede product performance.

WARNING

A warning is intended to alert the user to the presence of potentially harmful circumstances and provide precautionary guidance for mitigating risk of personal injury and or damage to the product.

NOTE

A note is a statement that clarifies or is used to emphasize important information.

1. Read all instructions

2. Keep these instructions for future reference.

3. Follow all instructions

4. Heed all warnings.

5. Do not submerge this apparatus in liquid of any kind.

6. Clean per recommended instructions using dry non-abrasive cloth.

7. Do not install near any sources of intense heat such as radiators, furnaces, stoves or other apparatus that regulary produce excessive heat.

8. Refer all servicing to qualified service personnel

1 SCOPE

This document describes the electrical interfaces for the Tamarisk®320 line of 17µm, LWIR OEM Modules and unless otherwise noted, this document describes all configurations of the module. Software and mechanical support documentation are described in separate documents See *Reference Documentation* for a complete listing.

The Tamarisk®320 product name identifies a family of long-wave infrared video cameras with a 17um pixel pitch 320 x 240 sensor array and comes in two basic configurations (Base and Base + Feature Board). Refer to the Tamarisk®320 Users Manual for more information.

In this section, the electrical interfaces for the Base configuration and Base + Feature Board configuration are described.
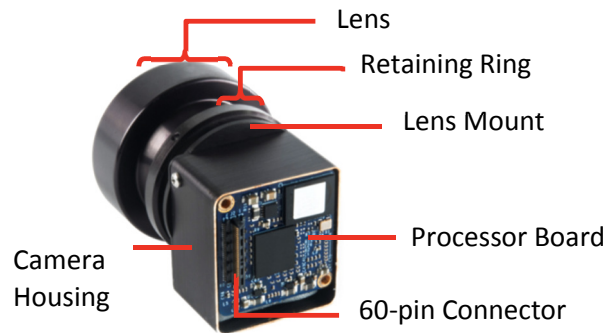

Figure 1: Tamarisk®320 Base Configuration

The Base configuration provides digital outputs in the form of 8-bit, 14-bit or "YUV Superframe" parallel digital video (LVCMOS UART), 8-bit, 14-bit, 24-bit RGB or "YUV Superframe" Camera Link® video, and supports shutter status through a 60-pin connector. Advantages of the Base configuration include parallel digital video output, reduced size, weight and power requirements.
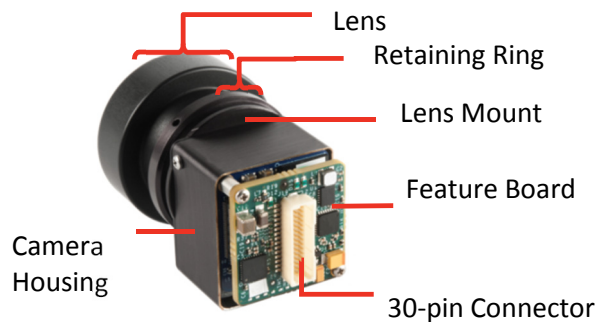
Figure 2: Tamarisk®320 Base + Feature Board Configuration

The Base + Feature Board configuration supports RS232 and USB 2.0 serial control, NTSC and PAL analog video outputs, digital video output via Camera Link® and accepts a range of input power voltages from 5-18V through a single 30-pin connector. Advantages of this configuration is that it provides analog video output, as well as full RS232 or USB 2.0 communication.

The recommended screw to secure the feature board is a .060-80 X .125 pan head screw.

2 ELECTRICAL INTERFACES

2.1 BASE CONFIGURATION ELECTRICAL INTERFACE

This configuration has no Feature board; the electrical interface is through a 60-pin connector located on the Processor board see Figure 1: Tamarisk®320 Base Configuration for location. A Board layout is provided below. For more dimesional information, please refer to Document No: 1003727 Tamarisk®320 Mechanical Interface Control Document. The Tamarisk Camera Link®[1] video, digital video, LVCMOS UART interface, shutter status are supported. See the electrical interface pin-out listed in Table 1.
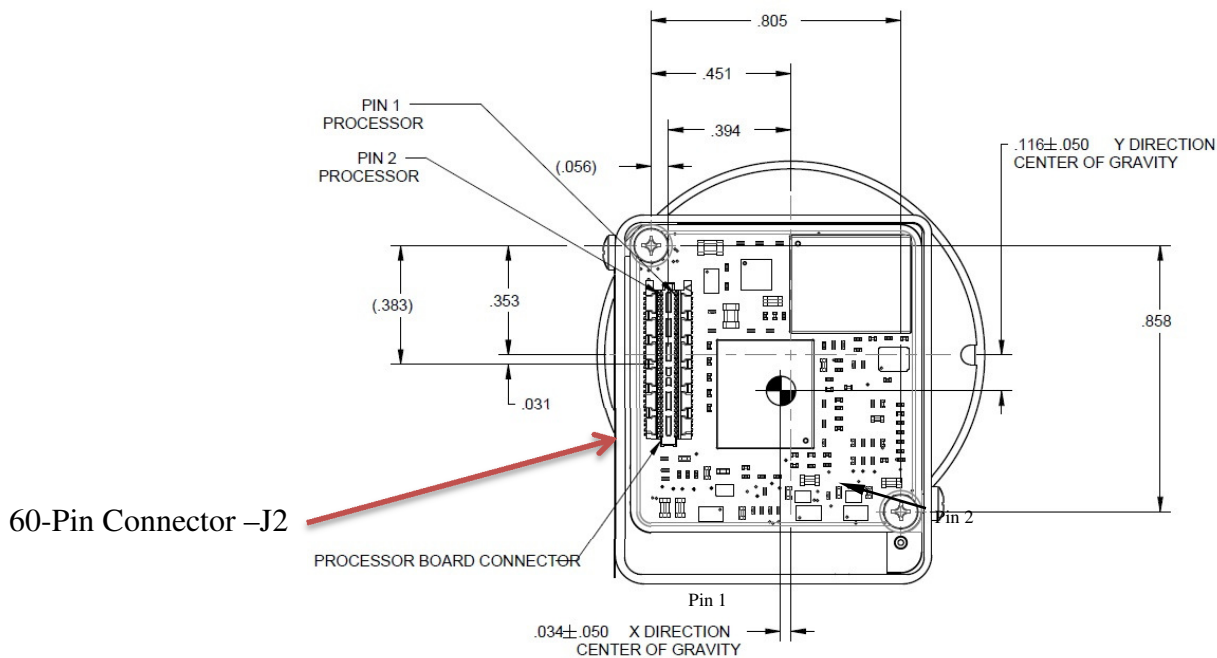

Figure 3: Processor Board with Connector Location and Dimensions

Table 1: Electrical Interface Pin-Out for Base Configuration

Pin	Signal Name	Func-tion	Description	Pin	Signal Name	Func-tion	Description
J2.1 J2.3 J2.5 J2.7	Ground	Power	Primary ground return for module power.	J2.2 J2.4 J2.6 J2.8	VIN	Power	Primary voltage supply for the camera/module (3-5.5V)
J2.9 J2.11	Reserved Reserved	NA	No Connection	J2.10	NC	NA	NA

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[1] Camera Link® serial control (LVDS_RDp/LVDS_RDn, LVDS_TDp/LVDS_TDn) are NOT supported in any configuration, serial control is always provided with the UART control for base configuration.

Pin	Signal Name	Func-tion	Description	Pin	Signal Name	Func-tion	Description
J2.13 J2.15	Reserved Reserved	NA	No Connection	J2.12	USB_DETECT	Input	USB Control signal detection. It is recommended that If communicating to the camera via a USB to serial converter, tie this pin low. If communicating to the camera via RS232 or another UART, tie this pin high.
J2.17 J2.19	LVDS_D3p LVDS_D3n	Output [2]	LVDS Video output Data 3	J2.14	UART_TX	Output	UART Control Output
J2.21 J2.23	LVDS_D2p LVDS_D2n	Output	LVDS Video output Data 2	J2.16	UART_RX	Input	UART Control Input
J2.25 J2.27	LVDS_D1p LVDS_D1n	Output	LVDS Video output Data 1	J2.18	Reserved	NA	No Connection
J2.29 J2.31	LVDS_D0p LVDS_D0n	Output	LVDS Video output Data 0	J2.20	Reserved	NA	No Connection
J2.33 J2.35	LVDS_CLKp LVDS_CLKn	Output	LVDS Video Data output Clock	J2.22	Reserved	NA	No Connection
J2.37	BDSI_D11	Output	Parallel Digital Data Output	J2.24	SHUTTER_DRIVE	Output	High when the shutter is driven
J2.39	BDSI_D10	Output	Parallel Digital Data Output	J2.26	SHUTTER_EVENT	Output	High during a calibration event
J2.41	BDSI_D9	Output	Parallel Digital Data Output	J2.28	Reserved	NA	No Connection
J2.43	BDSI_D8	Output	Parallel Digital Data Output	J2.30	Reserved	NA	No Connection
J2.45	BDSI_D7	Output	Parallel Digital Data Output	J2.32	Reserved	NA	No Connection
J2.47	BDSI_D6	Output	Parallel Digital Data Output	J2.34	Reserved	NA	No Connection
J2.49	BDSI_D5	Output	Parallel Digital Data Output	J2.36	Reserved	NA	No Connection
J2.51	BDSI_D4	Output	Parallel Digital Data Output	J2.38	GENLOCK	Input/ Output	Video Genlock signal master or slave. If not used, leave floating
J2.53	BDSI_D3	Output	Parallel Digital Data Output	J2.40	BDSI_PCLK	Output	Parallel Digital Video Clock
J2.55	BDSI_D2	Output	Parallel Digital Data Output	J2.42	BDSI_LSYNC	Output	Parallel Digital Video Line Sync (Active High)

[2] Unused outputs can be no connects
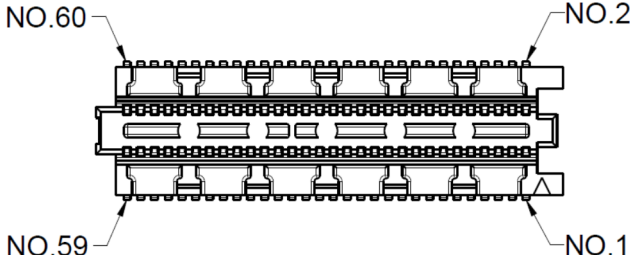"No connection" should be left floating.

Pin	Signal Name	Func-tion	Description	Pin	Signal Name	Func-tion	Description
J2.57	BDSI_D1	Output	Parallel Digital Data Output	J2.44	BDSI_FSYNC	Output	Parallel Digital Video Frame Sync (Active High)
J2.59	BDSI_D0	Output	Parallel Digital Data Output	J2.46	BDSI_D13	Output	Parallel Digital Video Data Output
J2				J2.48	BDSI_D12	Output	Parallel Digital Video Data Output
				J2.50 J2.52 J2.54	VCC_IO	Power Output	1.8V I/O Supply Output
				J2.56 J2.58 J2.60	Ground	Power	Ground

Figure 4: 60-pin Connector – J2

Figure 3 provides the board, mounting hole, and connector (J2) dimensions. All dimensions are in mils and all dimensions are show at the center of the connector or mounting holes (please see mechanical ICD listed in reference documentation for all up to date dimensions and drawings).

2.2 BASE CONFIGURATION INPUT POWER SPECIFICATION

The primary voltage input (VIN) for this configuration requires the input voltage to be within the range from 3.0 to 5.5VDC.   There are many readily available commercial power supplies power adapters, and or batteries/battery packs meeting this voltage range with the current requirements outlined in Table 2.

Table 2: Base Configuration Input Power Specification

Parameter	Description	Min	Typ	Max	Units
VIN	Input Voltage	3.0	5.0	5.5	V
Icc	Input Current (VIN=5.0)		200	260	mA
Icc with Shutter active*	Input Current RMS during transition (VIN=5.0)		400	650	mA
V_{OH} LVDX_XXX	V_{OH} High Level Output (2.5V output), I_{OH} = -1mA	2.0			V
V_{OL} LVDS_XXX	V_{OL} Low Level Output (2.5V output), I_{OL} = -1mA			0.4	V
V_{OH} UART_TX	V_{OH} High Level Output (1.8V output)	1.35			V
V_{OL} UART_TX	V_{OL} Low Level Output (1.8V output)			0.45	V
V_{IH} UART_RX, GENLOCK	V_{IH} High Level Input (1.8V input)	1.17		2.25	V
V_{IL} UART_RX, GENLOCK	V_{IL} Low Level Input (1.8V input	-0.3		0.63	V
V_{OH} BDSI®_xx, USB_DETECT,	V_{OH} High Level Output (1.8V output), I_{OH} = -2mA	1.35			V

Parameter	Description	Min	Typ	Max	Units
SHUTTER_DRIVE, SHUTTER_EVENT, WE_TEST#, GENLOCK					
V_{OL} BDSI_xx, USB_DETECT, SHUTTER_DRIVE, SHUTTER_EVENT, WE_TEST#, GENLOCK	V_{OL} Low Level Output (1.8V output), I_{OL} = -2mA			0.45	V

* The shutter is typically active for 100 mS closing and 100ms opening.

NOTE

Shutter current demand is instantaneous; care should be taken to provide bypass capacitance to prevent voltage regulator sag.

The module also provides a 1.8V output that can be used to supply some circuitry on the feature board for the system. This supply is used to drive all 1.8V outputs from the module.

Table 3: Base Configuration External 1.8V Drive Capability

Parameter	Description	Min	Typ	Max	Units
VCC_IO	I/O Output Voltage	1.71	1.8	1.89	V
Iout	Output Current			50	mA

2.3 BASE + FEATURE BOARD CONFIGURATION ELECTRICAL INTERFACE

The Base + Feature Board configuration supports RS170(NTSC and PAL), Camera Link®[1], RS232, USB, and various input power connection options. Electrical interface is through a 30-pin connector located near the center of the Feature board, See Figure 2. The electrical interface pin-out for this connector is detailed in Table 4 below:

Table 4: Electrical Interface for Base and Base +Feature Board Configurations

Pin	Signal Name	Function	Description
J19.1 J19.3	EXTPWR	Power	External Power input 5-18V
J19.5 J19.7	EXTPWR_GND	Power	External Power input ground
J19.2	RS232_RX	Input	RS232 input signal

| Pin	Signal Name	Function	Description
J19.4	RS232_TX	Output	RS232 output signal
J19.6	12V_CL	Power	12V power input
J19.8	GND_CL	Power	12V power input ground
J19.9 J19.11	USBDP USBDM	Bi-directional	USB Interface
J19.10 J19.12	LVDS_D0n LVDS_D0p	Output	LVDS Video Data output Data 0
J19.14 J19.16	LVDS_D1n LVDS_D1p	Output	LVDS Video Data output Data 1
J19.18 J19.20	LVDS_D2n LVDS_D2p	Output	LVDS Video Data output Data 2
J19.22 J19.24	LVDS_CLKn LVDS_CLKp	Output	LVDS Video Data output Clock
J19.26 J19.28	LVDS_D3n LVDS_D3p	Output	LVDS Video Data output Data 3
J19.30	A_VID_OUT	Output	Analog Video Output (RS-170 or NTSC or PAL)
J19.13	USB_5V	Power	USB 5V input power
J19.15	Ground	Power	Ground
J19.17 J19.19	NC NC	NA	NA
J19.21 J19.23	NC NC	NA	NA
J19.25	GENLOCK	Bi-directional	Video genlock signal master or slave
J19.27	Ground	Power	Ground
J19.29	Analog Video Ground	Power	Dedicated Analog Video Ground
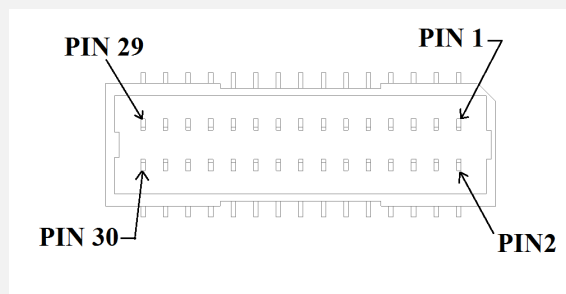
Figure 5: 30-pin Connector – J19

 Camera Link® serial control (LVDS_RDp/LVDS_RDn, LVDS_TDp/LVDS_TDn) are NOT supported in any configuration, serial control is always provided with the UART control for base + feature board.

2.4 BASE + FEATURE BOARD CONFIGURATION INPUT POWER SPECIFICATION

There are three ways to supply input power to this configuration; these are detailed in Table 5 below:

Table 5: Configuration 2 Input Power Specification

Input	Parameter	Description	Min	Typ	Max	Units
EXTPWR	VIN	Input Voltage	4.5	5.0	18	V
	Icc	Input Current (VIN=5.0)		220	280	mA
12V_CL	VIN	Input Voltage		12.0		V
	Icc	Input current		92	117	mA
USB_5V	VIN	Input Voltage		5.0		V
	Icc	Input Current		220	280	mA
Icc w/Shutter active*	Icc	Input Current RMS during transition (VIN=5.0)		400	650	mA
GENLOCK		V_{OH} High Level Output (1.8V output)	1.35			V
		V_{OL} Low Level Output (1.8V output)			0.45	V
GENLOCK, USB_5V		V_{IH} High Level Input (1.8V input)	1.17			V
		V_{IL} Low Level Input (1.8V input			0.63	V
RS-232 I/O		V_{OH} High Level Output	5			V
		V_{OL} Low Level Output			-5	V
		V_{IH} High Level Input	2.5		25	V
		V_{IL} Low Level Input	-25		0.8	V
LVDS_xxx		V_{OH} High Level Output (2.5V output), I_{OH} = -1mA	2.0			V
		V_{OL} Low Level Output (2.5V output), I_{OL} = -1mA			0.4	V
USBDP USBDM		V_{OH} High Level Output	2.8		3.6	V
		V_{OL} Low Level Output	0		0.3	V
		Single Ended Rx Threshold	0.8		2.0	V
		Differential Common Mode	0.8		2.5	V
		Differential Input Sensitivity	0.2			V
		Driver Output Impedance			44	ohms

* The shutter is typically active for 100 mS closing and 100ms opening.

NOTE

Shutter current demand is instantaneous; care should be taken to provide bypass capacitance to prevent voltage regulator sag.

Figure 6 illustrates the Feature Board's different power inputs (on the left) and the 5 Volt output (on the right) which is an input to the Processor Board. By design, the Feature Board accommodates a range of DC input voltage from 5 to 18V on EXTPWR. However, only one power input should be used at a time. The 5V to 18V regulator utilizes a Texas Instruments TPS61170DRVR.
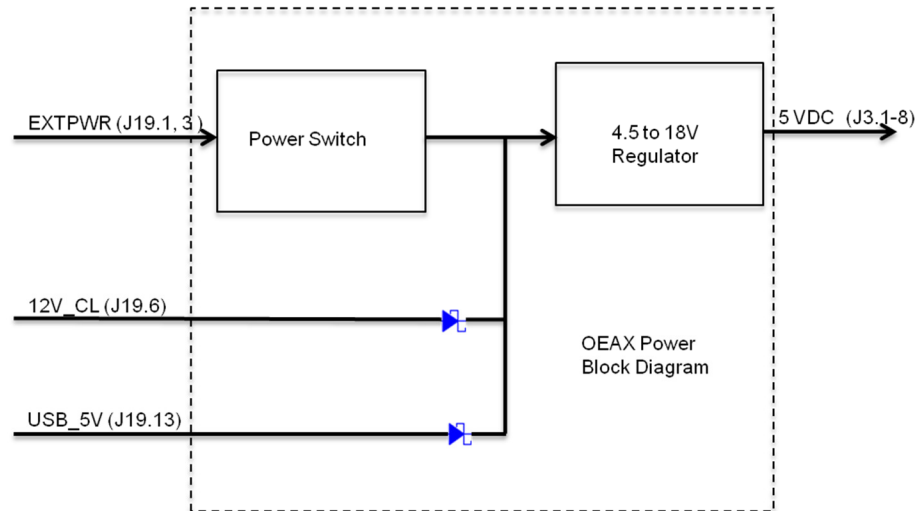

Figure 6: OEAX Board Power Block Diagram

2.5 UART INTERFACE

Command & Control for the module is handled through a standard UART. The interface to the UART is through the connectors described in Table 2 and Table 6. For base configuration the UART interface uses 1.8V CMOS logic levels, for base + feture board configuration the full RS-232 voltage levels are supported.

Table 6: UART Signal Definition Configuration 1 and 2

Configuration	Signal	Description
Base	UART_TX	UART Transmit Data. 1.8V LVCMOS output.
Base	UART_RX	UART Receive Data. 1.8V LVCMOS input. 3.3V tolerant. (NOT 5V tolerant)
Base + Feature	RS232_TX	UART Transmit Data. Supports full +/- 5V levels
Base + Feature	RS232_RX	UART Receive Data. Supports full +/- 25V input levels

2.6 SHUTTER CONTROL

If an external shutter is desired, two external signals are provided via base configuration 60-pin connector and base configuration + feature board's 30 pin connector. The SHUTTER_DRV signal is high when the shutter is being driven (open or closed) and low when the shutter is not driven. The SHUTTER_EVENT signal is high during a calibration event; this signal is used to indicate that the shutter is blocking the FPA. During normal operation the SHUTTER_EVENT signal is low. Refer to the shutter timing diagram for timing information.

2.7   GENLOCK

The GENLOCK signal in both base and base + feature board support frame linking to an external signal. All frame data will start based on the rising edge of the GENLOCK signal. Extra line syncs will be generated to avoid row burn out until the next rising edge of the GENLOCK signal.

GENLOCK will also support a master mode of operation where the camera system drives a frame sync to other components or subsystems via the GENLOCK pin.

When GENLOCK is configured in slave mode the frame rate can vary between >0 and 60Hz. Calibration times will increase at lower frame rates. (A frame rate of 0 Hz is a special case and can cause unexpected behavior during calibration.) The GENLOCK input signal high time can be as low as 1% and us much as 99% of the 60Hz frame time of 16.66mS(166uS to 16.5mS).

When GENLOCK is configured in master mode the GENLOCK signal goes high for at least 50nS once a frame.

For more information on how to set GENLOCK mode please see Document No: 1012819 Tamarisk®₃₂₀ Software Interface Control Document

2.8   USB_DETECT

Active low signal to indicate USB connection – NOT 5V tolerant in base configuration.

3 INTERFACES AND TIMING

Timing information for both the Base and Base + Feature Board configurations are described in this section.

3.1 LVDS INTERFACE

The LVDS interface supports two modes of operation Camera Link mode and YUV Superframe mode.

Camera Link®mode is typically used to interface to Camera Link® frame grabbers. The LVDS video interface supports 4 LVDS data pairs and the LVDS clock pair as outputs.   The LVDS timing is shown in Table 7, while the timing diagram is shown in Figure 7 and Figure 8. The LVDS Clock signal has a non fifty percent duty cycle. It is based on a 7x internal clock. The LVDS Clock is high for 4 of the 7x clock periods and low for 3. During each clock period 7 bits are transmitted on each data pair. The bits are transmitted in the order shown in Figure 7 with each pixel value starting in the middle of the high clock period. The LVDS data window timing is shown in Figure 8. The maximum delay for the data to become valid after clock and the minimum time data will go invalid before the clock are also described in Table 7.

Table 7: LVDS Timing and Framing

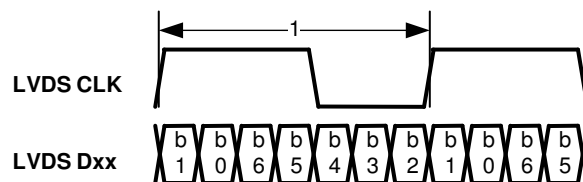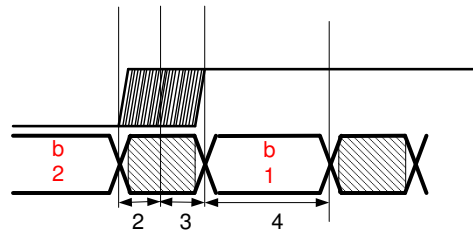| Number	Parameter	Min	Nom	Max	Units
1	Clock Period		48.6		ns
	7x Internal Clock Freq		144		MHz
	Bit time		6.94		ns
2	Data no longer valid before clock			0.4	ns
3	Clock to data valid			0.4	ns
4	Data valid window	6.14			ns
#LINES	Lines per frame		480		
#PIXELS_CL	Pixels per line in Camera Link Mode		640		
#PIXELS_YUV	Pixels per line in YUV_SF mode		1280		

Figure 7: LVDS Format Diagram
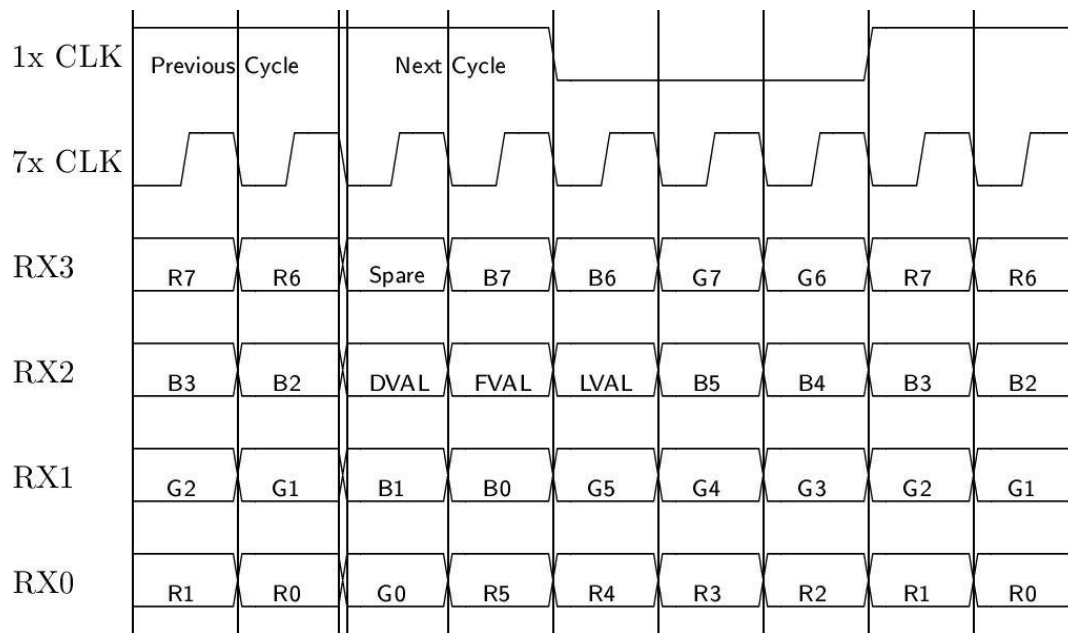
Figure 8 LVDS Timing Diagram

Figure 9 Camera Link® bit mapping for 24 bit RGB color

Figure 9, shows the mapping of Camera Link® serialized bit stream to 24 bit RGB color. FVAL is low (invalid) between frames while LVAL is low (invalid) between lines. DVAL is high to indicate that the data is valid. A frame will consist of FVAL going high (valid) for an entire frame. Blanking time is inserted between each frame while FVAL is low. A line will consist of LVAL going high (valid) for an entire line. Blanking time is inserted between each line while LVAL is low.   The amount of horizontal and vertical blanking can change based on operating modes and Camera revisions.

The LVDS Interface supports three interface formats:

1. 14/8 bit Gray Scale
2. 24 bit RGB
3. YUV_Superframe

The 14bit Gray Scale format is used to support the **14bit** and **8bit** gray scale data modes. The 14bit and 8bit Gray Scale mapping follows the Camera Link® standard and maps as shown in Table 8.
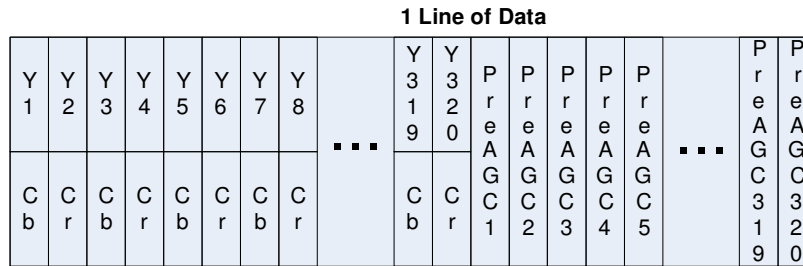
Table 8 Camera Link® Gray Scale and YUV_Superframe Mapping to 24 bit color map

Camera Link® 24 Bit color	14bit data mode	8bit data mode	YUV Superframe Mode
G7	Not Used	Not Used	Bit 15
G6	Not Used	Not Used	Bit 14
G5	Bit 13	Bit 7	Bit 13
G4	Bit 12	Bit 6	Bit 12
G3	Bit 11	Bit 5	Bit 11
G2	Bit 10	Bit 4	Bit 10
G1	Bit 9	Bit 3	Bit 9
G0	Bit 8	Bit 2	Bit 8
R7	Bit 7	Bit 1	Bit 7
R6	Bit 6	Bit 0	Bit 6
R5	Bit 5	Not Used	Bit 5
R4	Bit 4	Not Used	Bit 4
R3	Bit 3	Not Used	Bit 3
R2	Bit 2	Not Used	Bit 2
R1	Bit 1	Not Used	Bit 1
R0	Bit 0	Not Used	Bit 0

The 24bit RGB format is used to support the colorization data mode and uses the standard Camera Link® 24bit RGB format.

In YUV Superframe mode a 16 bit video stream is mapped into the Camera Link® Interface as shown in Table 8. The YUV Superframe consists of 240 lines with each line containing 640 values. The first 320 values contain YCbCr generated values for the pixels of that line with the second 320 values containing the pre-AGC values for that line (currently the pre-AGC values are from the frame before the current YCbCr frame, this allows time for analytics to analyze the pre-AGC data so additional overlays can be added to the YCbCr data stream by customer analytics). Figure 10 depicts a YUV Superframe line. The first Cb and Cr data is generated on the average of the first two pixels. The second Cb and Cr data is generated on pixels 3 and 4 with all further Cb/Cr pairs calculated in a relative manner. The Pre-AGC data is LSB aligned so if the Pre-AGC data is only 14 bits it will only occupy the lower 14 bits of the data path respectively.

For Tamarisk®320 Precision Series cameras, the Pre-AGC data is replaced with per pixel temperature data in 11.5 format. The 11.5 format is provided in Kelvin is defined as 11 bits of decimal temperature data with 5 bits of fractional data. See the user manual for the exact temperature calculation.

1 Line of Data

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	...	Y319	Y320	PreAGC1	PreAGC2	PreAGC3	PreAGC4	PreAGC5	...	PreAGC319	PreAGC320
Cb	Cr	Cb	Cr	Cb	Cr	Cb	Cr		Cb	Cr								

Figure 10 YUV Line Format

3.2 PARALLEL DIGITAL VIDEO INTERFACE

The digital video interface can operate in one of three modes:

1. Parallel Video mode,
2. RS-170 Video mode,
3. YUV Superframe mode.

The Parallel Video mode provides a pixel output clock, Line Sync, Frame Sync and 14-bit data. This mode is used to directly interface to another digital interface (i.e. a processor such as https://www.leopardimaging.com/Thermal_IP_Camera_Dev_Ki.html). The parallel digital video interface supports 8 or 14 bit digital video data. Any post-AGC selected video will be 8 bit data (MSB on BDSI_D13, LSB on BDSI_D6 from Table 1); Pre-AGC selected video will be 14 bit. For customers that require pre-AGC video, methods will be provided to select full 14 bit video data (see Document No: 1012819 Tamarisk®320 Software Interface Control Document).

The default Tamarisk® PDVO interface timing specifies 0.5ns of delay time following the rising edge of PCLK (see Figure 11 and Table 9). This design works well for designs that latch the data, frame sync, and line sync on the falling edge of PCLK.
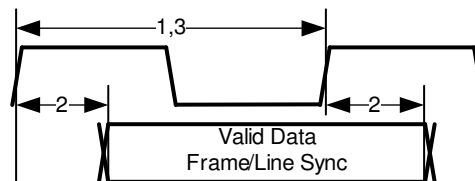
Figure 11: Default Parallel Digital Video Timing Diagram

Table 9: Default Parallel Digital Video Timing

Number	Parameter	Min	Nom	Max	Units
1	BDSI_PCLK clock frequency for 30 Hz/60Hz frame rate or 9Hz		10	40.5	MHz
2	Clock to Data/Fsync/Lsync valid after the rising edge of the clock	0.5		Clock period – 10	ns

| 3 | Period of BDSI_PCLK | | 100 | | ns |

Note: Data will be valid for 10 ns before the rising edge of the next clock.

Note: 30Hz for Tamarisk®640, 60Hz for Tamarisk®320

For applications which latch data, frame sync, and line sync on the rising edge of PCLK, DRS has added a non-volatile parameter. For customers who require additional hold time beyond the specified 0.5ns, a non-volatile parameter (NV PARAM # 197) has been provided to extend the hold time. Figure 12 illustrates the parallel digital video output timing when NV PARAM #197 is set to 1.
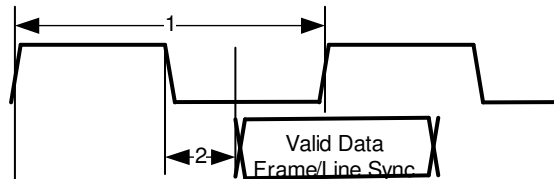
Figure 12: New Parallel Digital Video Timing Diagram

Table 10 through Table 12 shows the timing specification for alternate supported parallel digital video output modes.

Table 10 Parallel Digital Video Timing 14 or 8 bit data (NV Parameter 197 set to 1)

Number	Parameter	Min	Nom	Max	Units
1	BDSI_PCLK clock frequency for 30 Hz/60Hz frame rate or 9Hz		10		MHz
2	Output Delay for Data/Fsync/Lsync	-25		25	ns
Note: 30Hz for Tamarisk®640, 60Hz for Tamarisk®320					

Table 11 Parallel Digital Video Timing RS-170 data (NV Parameter 197 set to 1)

Number	Parameter	Min	Nom	Max	Units
1	BDSI_PCLK clock frequency for 30 Hz/60Hz frame rate or 9Hz		27		MHz
2	Output Delay for Data/Fsync/Lsync	-9		14	ns
Note: 30Hz for Tamarisk®640, 60Hz for Tamarisk®320					

Table 12 Parallel Digital Video Timing Superframe™ data (NV Parameter 197 set to 1)

Number	Parameter	Min	Nom	Max	Units
1	BDSI_PCLK clock frequency for 30 Hz/60Hz frame rate or 9Hz		40.5		MHz

2	Clock to Data/Fsync/Lsync setup time before edge of clock	-8		10	ns
Note: 30Hz for Tamarisk®640, 60Hz for Tamarisk®320					

Figure 13 illustrates the Parallel Digital Interface's horizontal timing. The BDSI_LSYNC signal will go high for 320 clocks each line to indicate valid video data is available via the data bus (BDSI_DATA). The BDSI_LSYNC signal will go low for several BDSI_PCLKs between each line of data. The number of clocks the BDSI_LSYNC is low between valid lines (horizontal blanking time) can vary based on the operating mode and camera release.
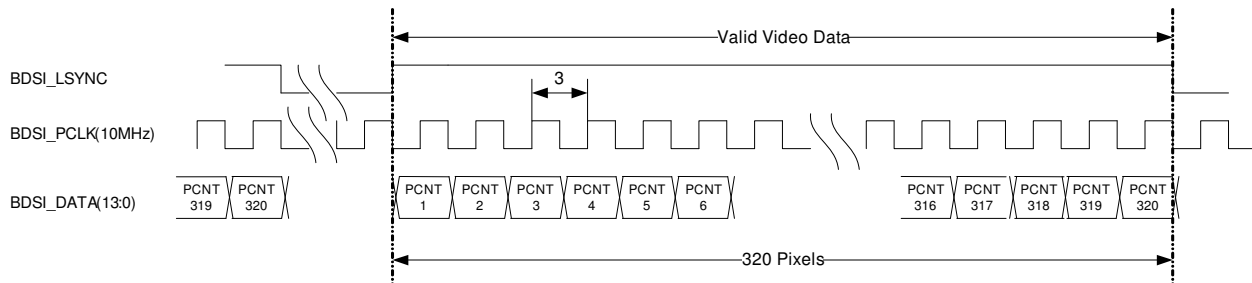
Figure 13: Parallel Digital Video Horizontal Timing Diagram

Figure 14 illustrates the Parallel Digital Interface's vertical timing. The BDSI_FSYNC signal will go low between each frame of video data to indicate that the next line of video received while the BDSI_FSYNC signal is high is the first line of the next video frame. The BDSI_FSYNC signal will go high at least one clock before the BDSI_LSYNC signal goes high (front porch). The BDSI_FSYNC signal will go low at least one clock after the BDSI_LSYNC signal goes low for the last line of a frame (back porch). It is intended for the user to sample these signals with the BDSI_PCLK signal. The vertical blanking time will vary between operating modes and camera release.
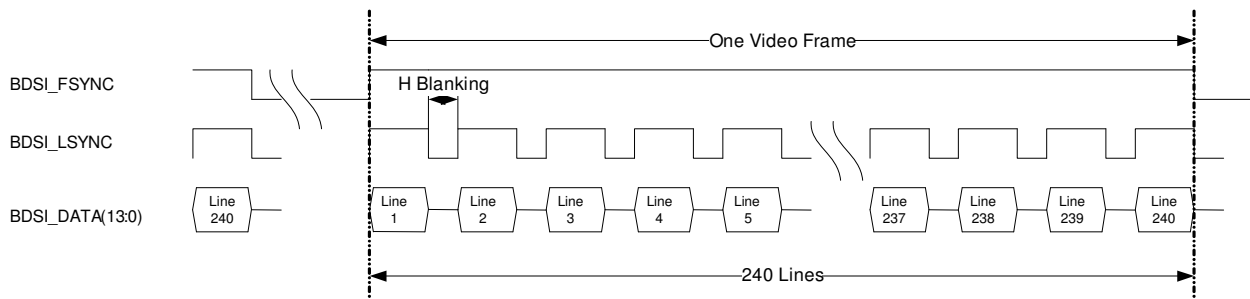

Figure 14: Parallel Digital Video Vertical Timing Diagram

The default mode on the base configuration will drive RS-170 digital encoding designed to drive a video codec – for example AD9705 digital to analog converter.   (Note: This mode is not recommended for users that are not planning on driving a Digital to Analog converter.) The data will be contrived to generate a valid analog signal that conforms to the RS170 specifications. The output

analog signal adheres to requirements for RS170 NTSC, or one of three PAL modes (see Document No: 1012819 Tamarisk®320 Software Interface Control Document for information on how to set PAL modes). The 320x240 image data will be stretched in both directions to more completely fill an NTSC or PAL display.

Data is driven on BDSI_D9 through BDSI_D0 (10 bits). The data is binary format. BDSI_PCLK, provides the single ended clock for the D/A conversion at 27 MHz. Example timing is shown in Figure 15 and Figure 16 for PAL mode, and Figure 17 and Figure 18 for NTSC mode.
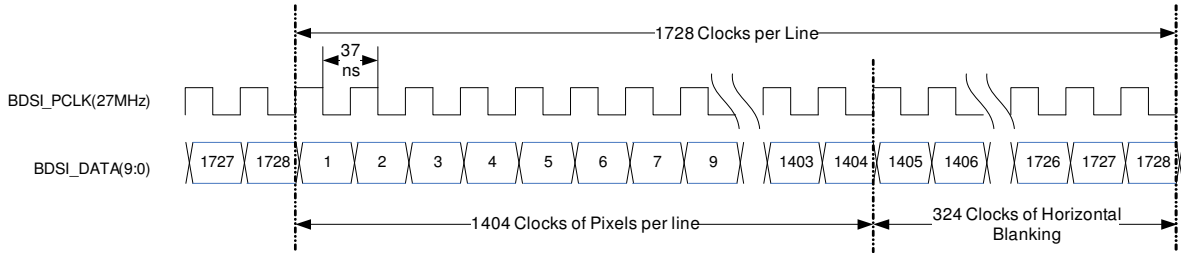
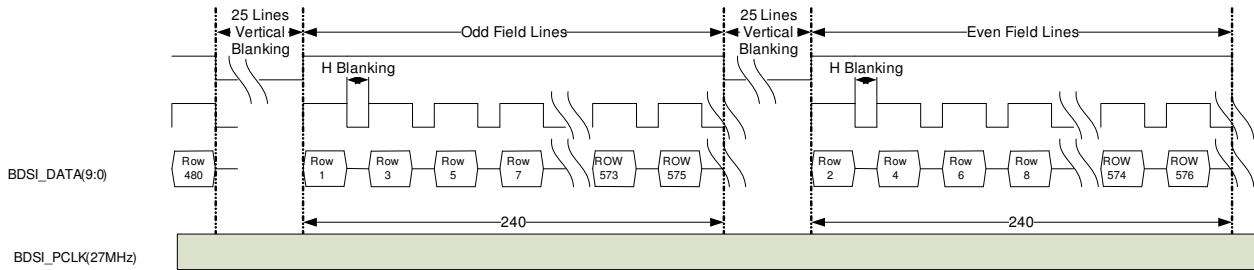Figure 15: Parallel RS-170 PAL Video Horizontal Timing Diagram

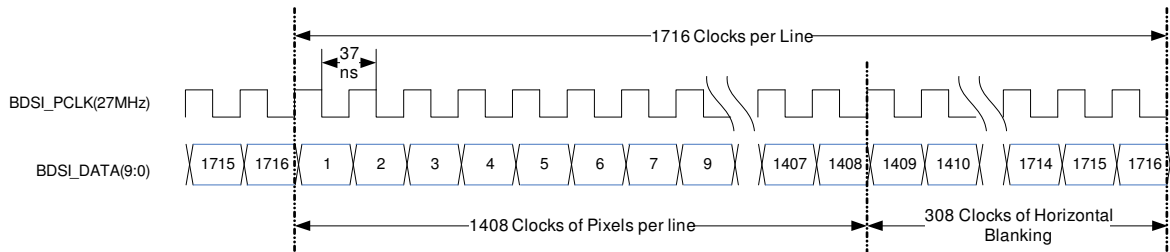Figure 16: Parallel RS-170 PAL Video Vertical Timing Diagram

Figure 17: Parallel RS-170 NTSC Video Horizontal Timing Diagram
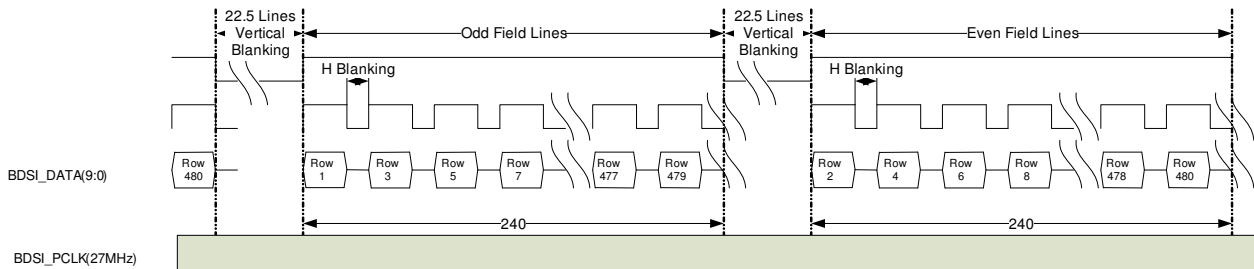

Figure 18: Parallel RS-170 NTSC Video Vertical Timing Diagram

In YUV_SuperFrame mode the Parallel Digital Video Interface is formatted with 1280 bytes per line and 240 lines per frame. The format of Parallel Digital Video Interface is shown in Figure 19 and Figure 20. Each line contains 320 Y values (one per pixel) interleaved with 160 Cb and 160 Cr values (Cb and Cr are calculated over 2 adjacent pixels) followed by the Pre-AGC data for the same line (The Pre-AGC data is the pixel data before any non-linear gains are applied). The format of the Pre-AGC data is 16 bits sent 8 bits at a time. The 8 bits occupy the bits 13 down to 6 of the BDSI bus with the most significant bit in bit 13 and the other bits filled in respectively. The lower 8 bits of a pixel are sent on one clock with the upper 8 bits being sent on the next clock. The 14 bits of raw data is converted to 16 bits that are LSB aligned – that is bits 15:14 will always be low. The lower byte of the 14bit raw data is sent first followed by the upper byte. The clock rate while in YUV SuperFrame mode is 40.5MHz. The amount of blanking time between lines and frames will vary based on camera mode and revision. The pre-AGC values are from the frame before the current YCbCr frame. This allows for signal processing on the pre-AGC values prior to enhancements being added to the YCbCr displayed to a user.

For Tamarisk®320 Precision Series cameras, the Pre-AGC data is replaced with per pixel temperature data in 11.5 format. The 11.5 format is provided in Kelvin is defined as 11 bits of decimal temperature data with 5 bits of fractional data. See the user manual for the exact temperature calculation.
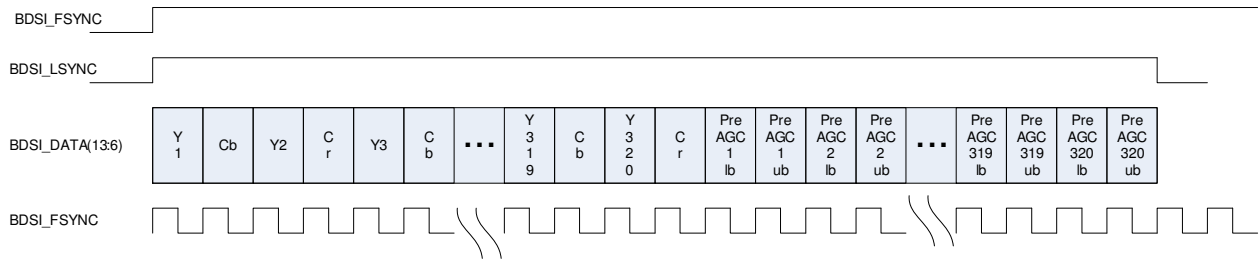

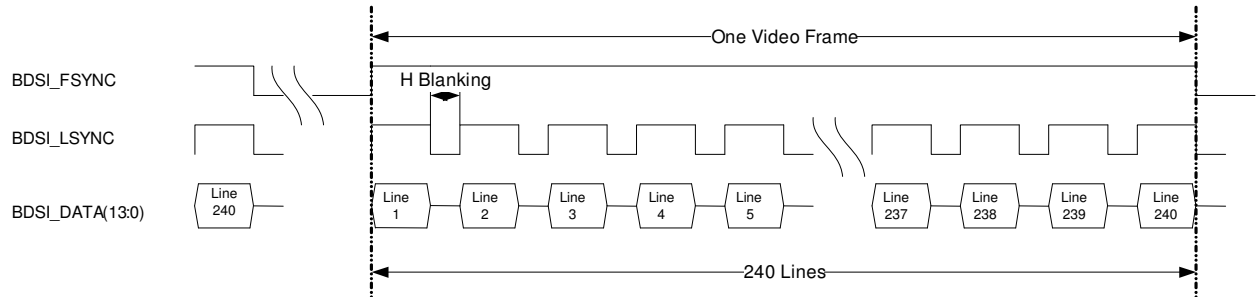Figure 19 YUV SuperFrame Line Format Over Parallel Digital Video Interface

Figure 20 YUV Sperframe Frame Format Over Parallel Digital Video Interface

Table 13: YUV_SuperFrame Video Timing

Number	Parameter	Min	Nom	Max	Units
1	BDSI_PCLK clock frequency for 60 Hz, 30 Hz frame rate or 9Hz		40.5		MHz
2	Clock to Data/Fsync/Lsync valid after the rising edge of the clock	0.5		Clock period – 10	ns
Note: Data will be valid for 10 ns before the rising edge of the next clock.					

3.3   ANALOG VIDEO INTERFACE

The camera provides an analog video output which follows the RS-170 standard (base + feature only). The analog video output signal is transmitted at 1v Peak-to-Peak.   Following are the nominal output signal levels when terminated with 75 Ohms (+/- 5%).

Sync tip   -0.284 V

Blank   0 V

Black   0.051 V

White   0.714 V

Frame timing parameters are shown in Table 14.

Table 14: Analog Video Timing

RS-170 Out				
Quantity	Description	Clocks	Rate	time
Pixel		1	13.5 MHz	74.074 ns
line	780 total pixels	858		63.556 us
line blanking	140 blanking pixels	144	15.734 kHz	10.700 us
active video	640 active pixels	640		47.400 us
field	262.5 lines	225,225		16.683 ms
vertical blanking	20 lines	17,160	61.050 Hz	1.271 ms
frame	525 lines	450,450		33.367 ms
vertical blanking	40 lines	34,320	30.525 Hz	2.542 ms
Active video	485 lines	416,130		30.824 ms

The camera's FPA outputs an image that has 240 lines that are stretched to 480 lines, but RS-170 specifies 485 lines of active video. The module accommodates this by inserting "black" lines in line positions 481 through 485 as illustrated in Figure 21.
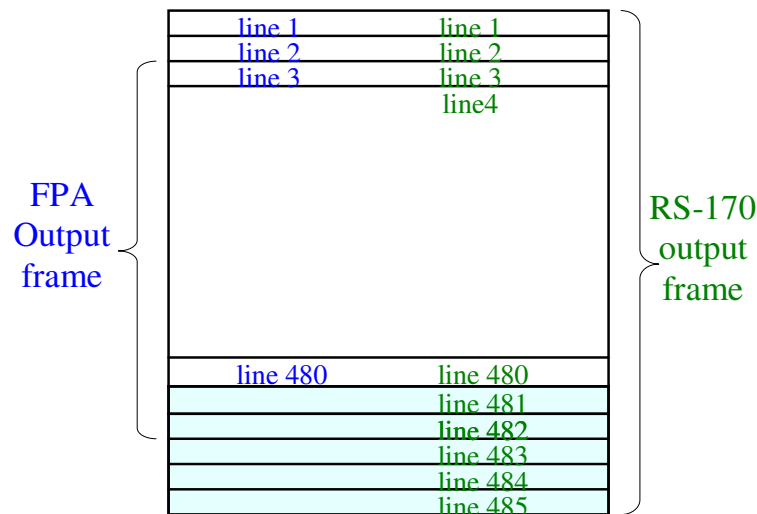

Figure 21: Analog Video Format

3.4   USB INTERFACE(BASE + FEATURE ONLY)

The USB interface utilizes FTDI's FT232RQ. The FT232RQ is a UART to USB Transceiver. For specific timing information refer to the FTDI data sheet.

3.5   RS-232 INTERFACE(BASE + FEATURE ONLY)

The RS-232 interface utilizes Linear Technologies' TC2801IDE#PBF. The TC2801IDE#PBF is a UART to RS-232 Transceiver. For specific timing information refer to the Linear Technologies data sheet.

3.6   SHUTTER INTERFACE

The shutter is not spring loaded. The shutter is bi stable. If the shutter is closed and the camera is powered down, the shutter will remain closed until power is applied again. If the shutter is open and the camera is powered down, the shutter will remain open.

The shutter timing diagram is shown in Figure 22. When the SHUTTER_EVENT signal is high, the camera's software is performing calibration. As the camera warms or cools the camera may change operating ranges. During these operating range changes, the shutter is closed for a longer period of time.

Table 15: Shutter Timing

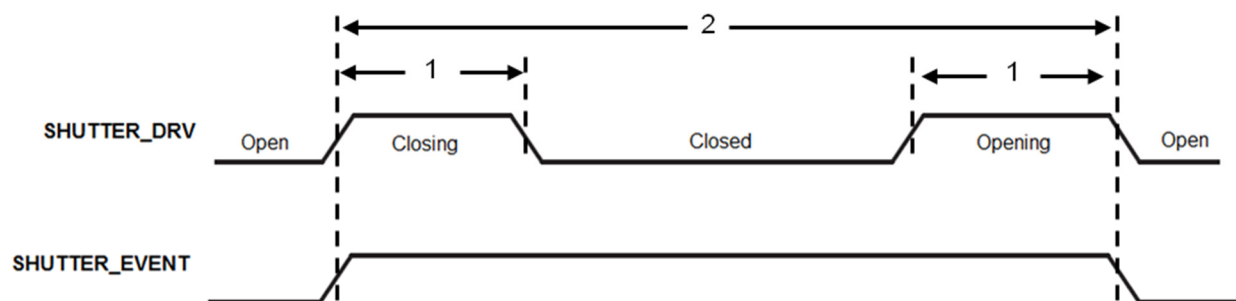| Number	Parameter	Min	Nom	Max	Units
1	SHUTTER_DRV high time		100		ms
2	SHUTTER_EVENT high time without a range change			440	ms
	SHUTTER_EVENT high time during a camera range change			1	s

Figure 22: Shutter Timing

4 ELECTRICAL CONNECTORS

There are two electrical connectors that support electrical interface to the Tamarisk®640 camera module, with the connector type being dictated by the model configuration. The connector manufacturer and part number shown below is the part number which is on the camera board. The designer must interface to one of these connectors. Please refer to the Tamarisk®640 Users Manual for more details:

Configuration 1: 60-pin Samtec ST4-30-1-L-D-P-TR. http://www.samtec.com/

Configuration 2: 30-pin JST BM30B-SRDS-G-TF. http://www.jst.com/index.html